

FIG. 2

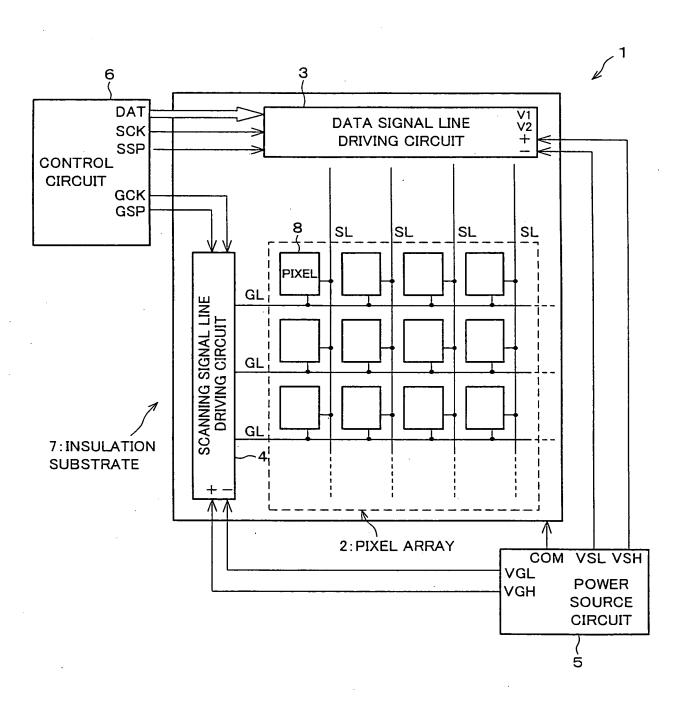


FIG. 3

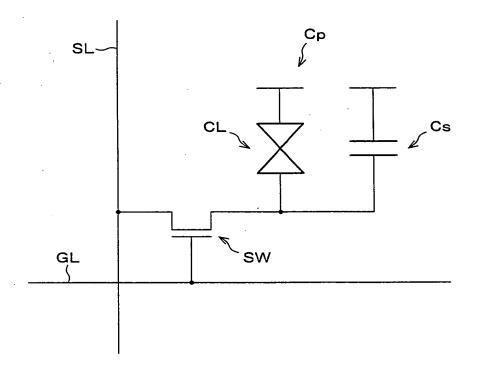


FIG. 4 (a)

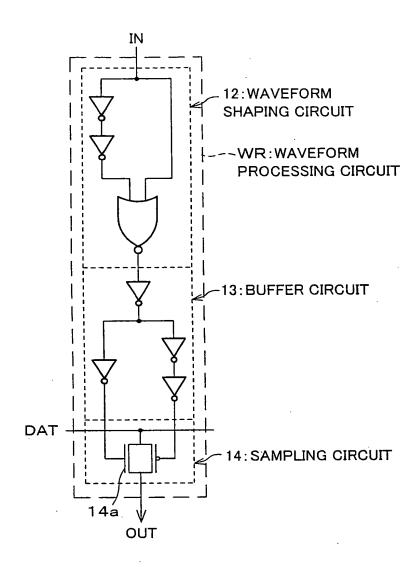
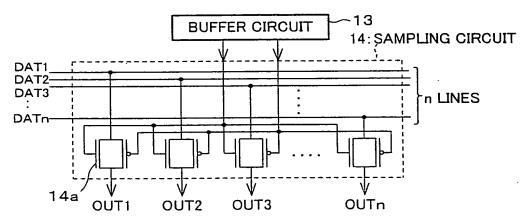
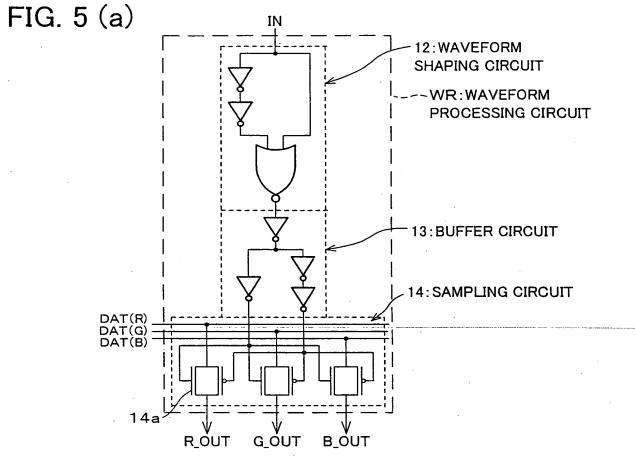
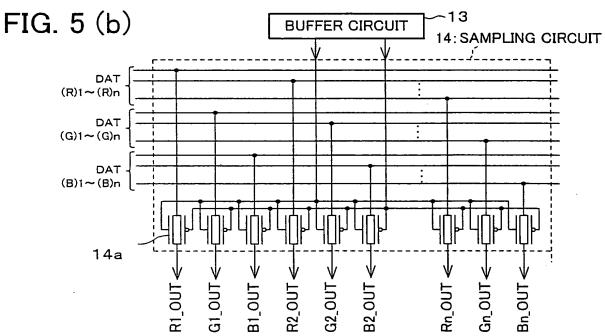


FIG. 4 (b)







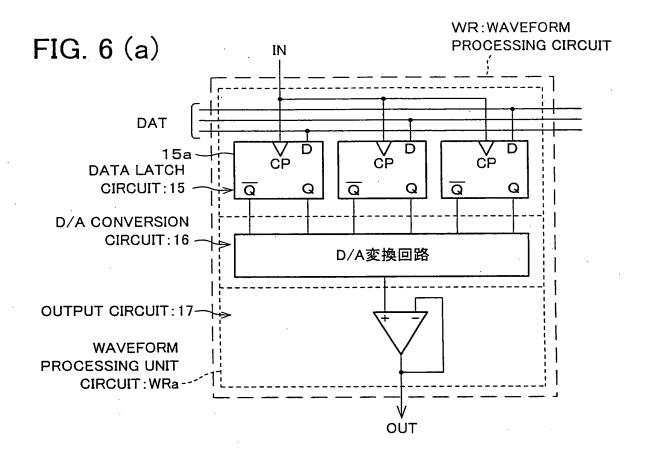


FIG. 6 (b)

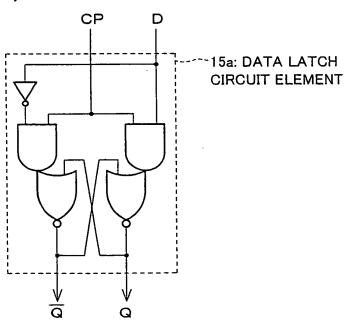


FIG. 7

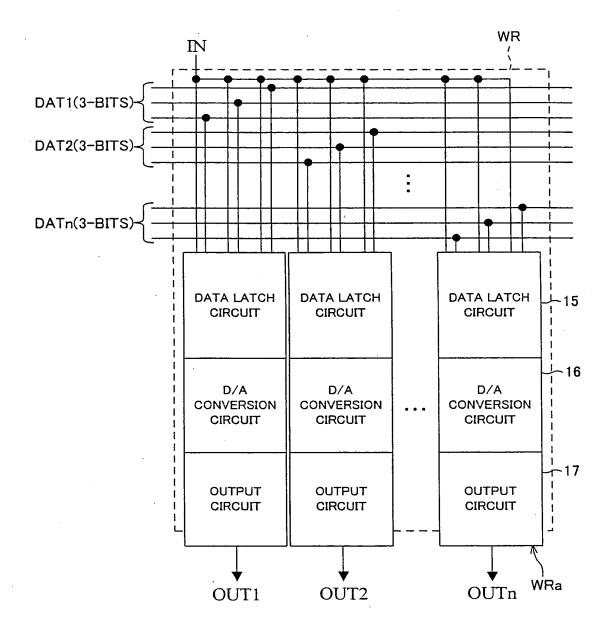
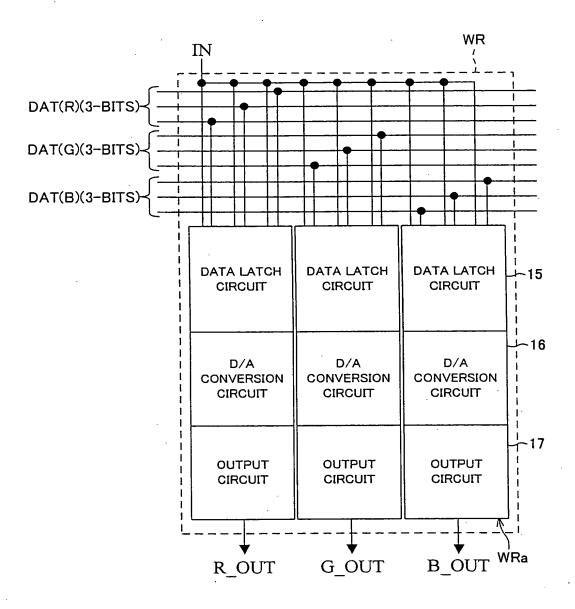
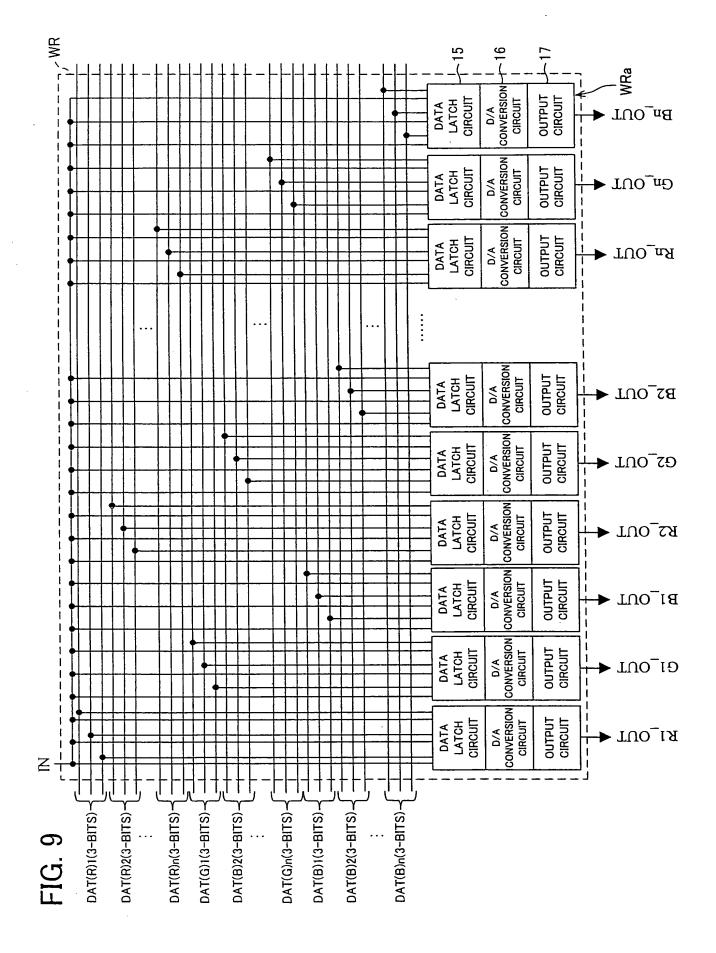
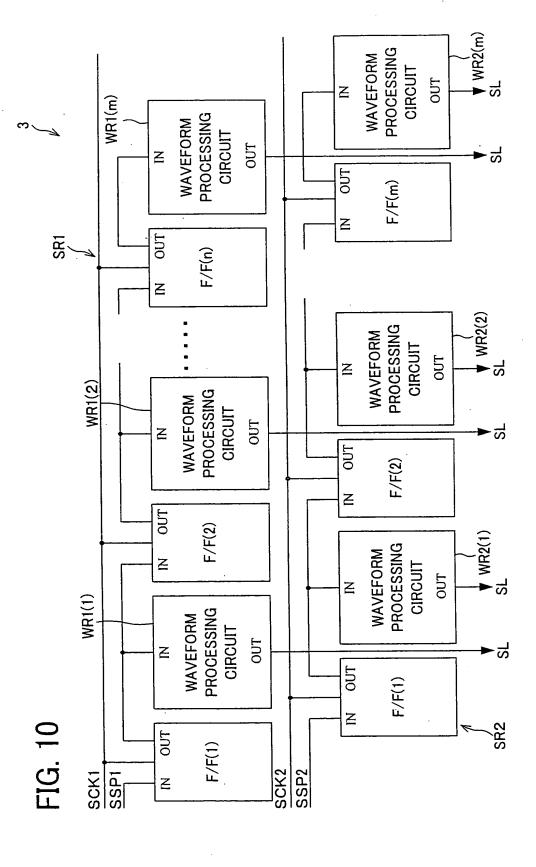
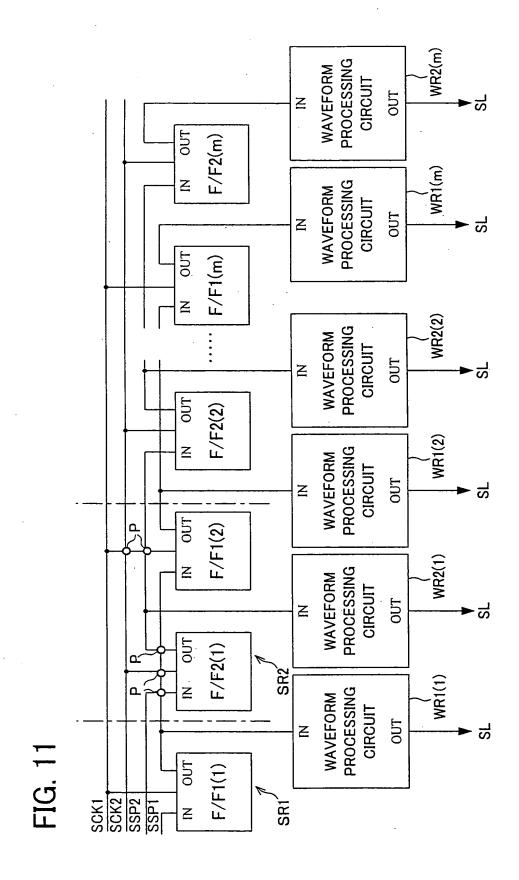


FIG. 8



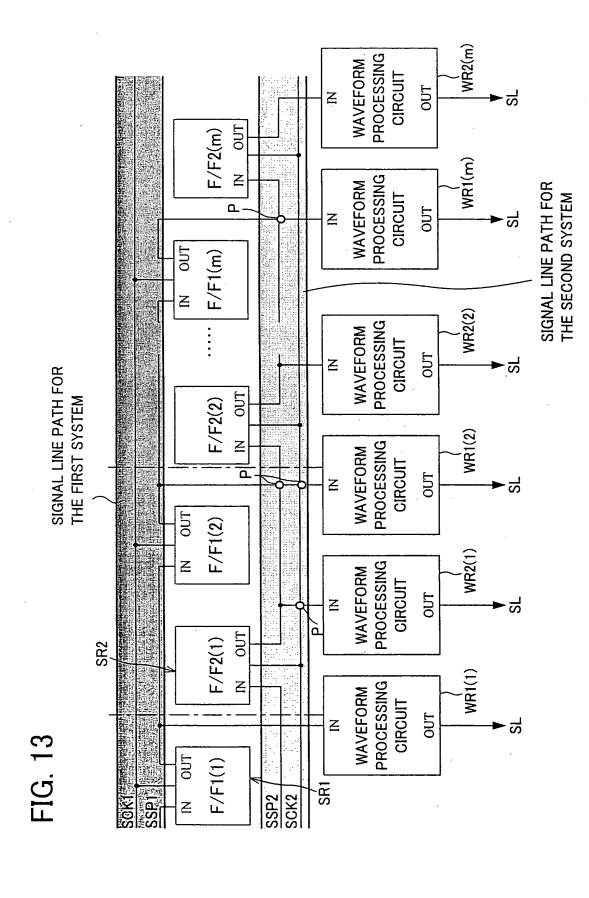


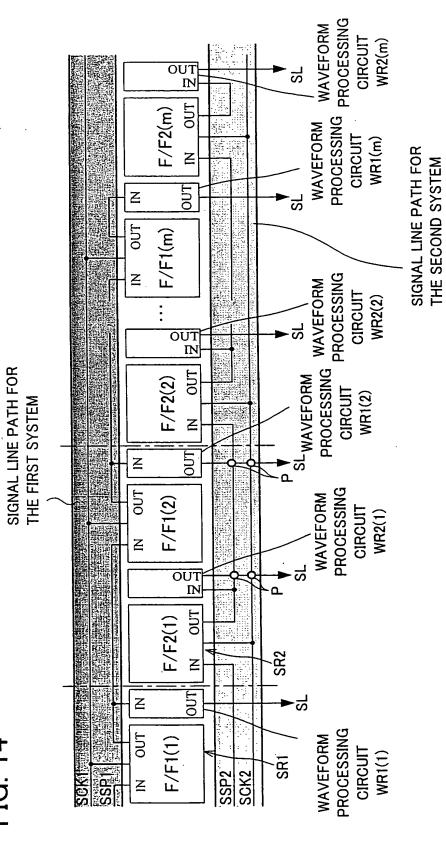




PROCESSING CIRCUIT WR2(m) WAVEFORM OUT Z OUT F/F2(m) PROCESSING WAVEFORM CIRCUIT WR1(m) Z OUT Z OUT F/F1(m) WAVEFORM PROCESSING CIRCUIT WR2(2) Z OUT Z WAVEFORM PROCESSING OUT F/F2(2)CIRCUIT WR1(2) OUT Z OUT WAVEFORM PROCESSING CIRCUIT WR2(1) F/F1(2)Z OUT Z OUT F/F2(1) PROCESSING CIRCUIT WR1(1) SR2 WAVEFORM Z OUT Z OUT F/F1(1) SCK2 SSP2 Z SR1 SCK1 SSP1

FIG. 12





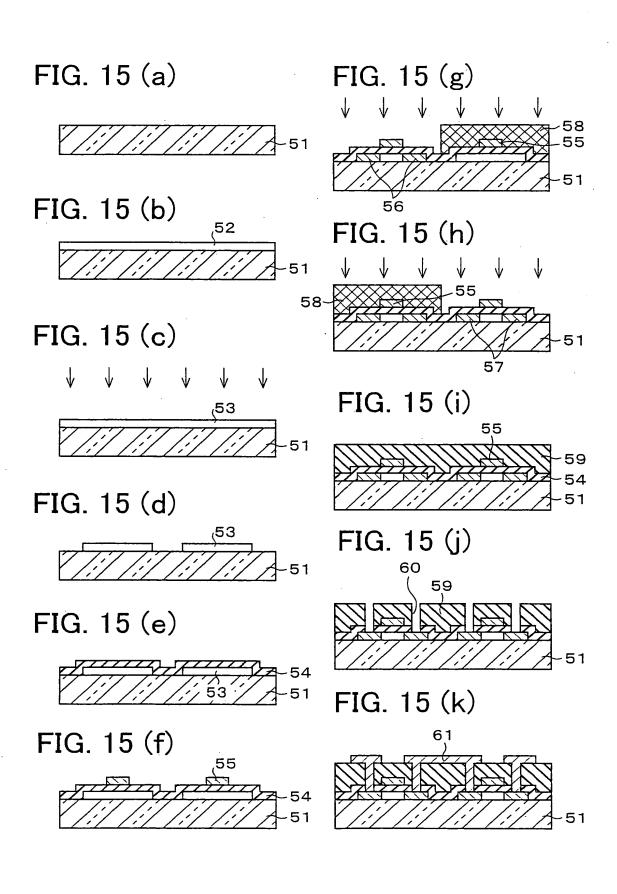
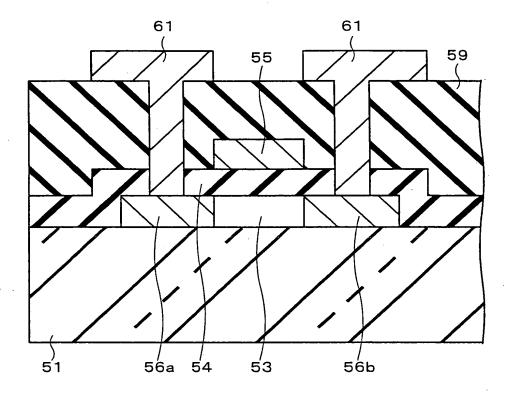
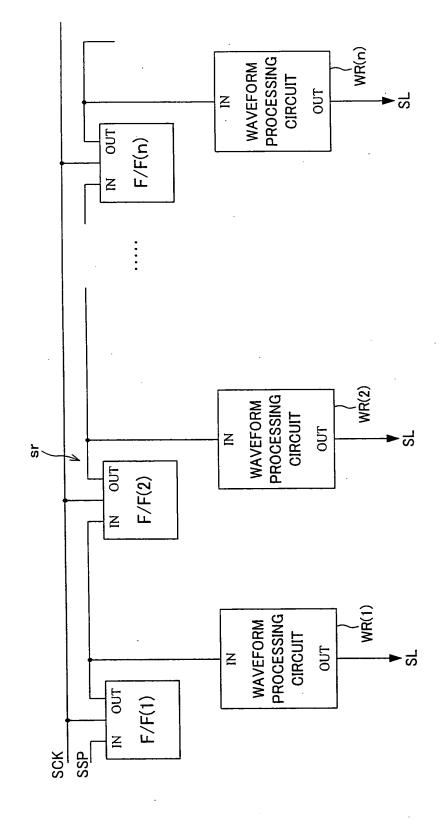
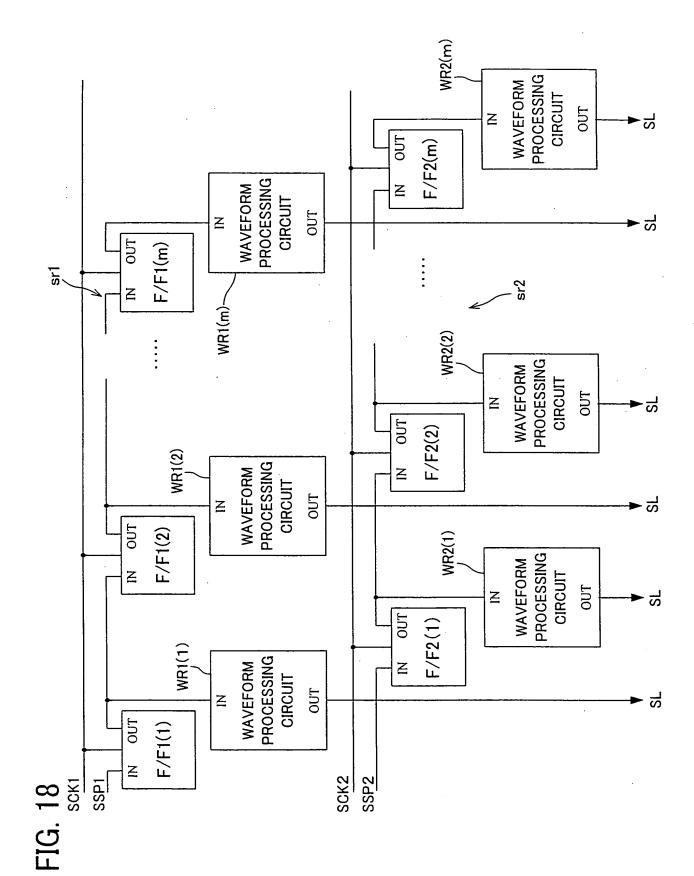


FIG. 16





-1<u>G</u>



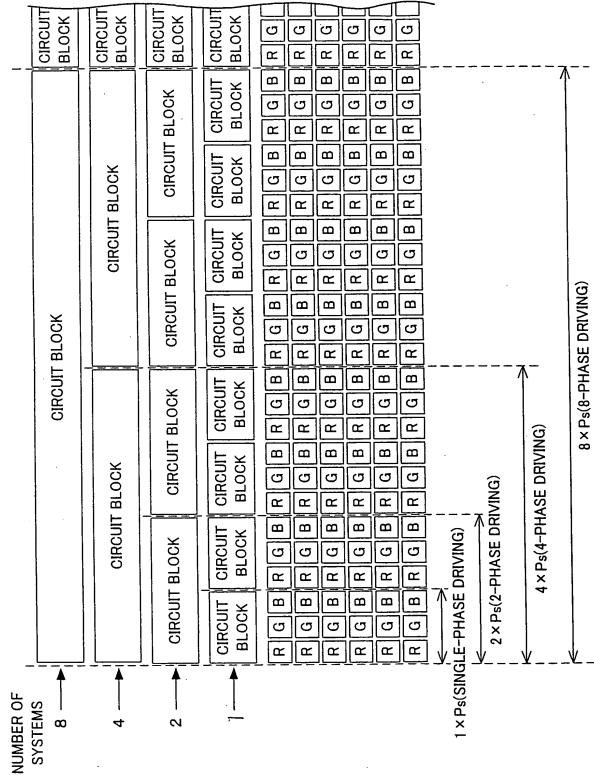


FIG. 20

